REMARKS

Examiner Graybill is thanked for the courtesies extended to the undersigned attorney during the personal interview conducted on July 28, 2004. Applicant's separate record of the substance of that interview is incorporated into the following discussion.

Claims 109, 111, 115, 116, 119, 120, 127 and 129-133 are pending. Applicants propose amendment of claims 109 and 111 to incorporate the features of claims 110 and 112, respectively, and cancellation of claims 110, 112, 123, 134 and 135. Accordingly, entry of the amendments after final rejection does not raise new issues.

Claims 109-112, 131, 134 and 135 were rejected under 35 USC §102(e) as being anticipated by Yasunaga et al. This rejection is respectively traversed.

Independent claims 109 and 111 have been amended to include the features that both a side portion of the resin layer and a side portion of the semiconductor element are respectively exposed. In this regard, the Office Action refers to a resin layer 121 and a side portion 109 of the semiconductor element 125. These features are illustrated in Figs. 98A-D of Yasunaga et al. However, on the other hand, in formulating the rejection of original claims 109 and 111, the Office Action relies on the embodiment illustrated in Fig. 96. The embodiments illustrated in Fig. 96 and Fig. 98A-D are different embodiments. See column 1, lines 62-64 which refers to Fig. 96 as disclosing an embodiment disclosed in Japanese Patent Laid-Open No. 3-104141 and column 2, lines 14-18 describing that Fig. 98 refers to an embodiment disclosed in Japanese Patent Lai-Open No. 4-207046. The embodiment illustrated in Figs. 98A-D does not contain the limitations required by independent claims 109 and 111. Conversely, the embodiment illustrated in Fig. 96 does not meet the limitations set forth in claims 110 and 112. As such, the Examiner's

anticipation rejection of these claims is without basis. Yasunaga et al. does not teach the features set forth in amended claims 109 and 111.

Independent claim 131 requires the compression-molded resin layer and the semiconductor element having surfaces defined by cutting using a dicer. Yasunaga et al. does not disclose a compression-molded resin layer wherein the compression- molded resin layer and the semiconductor element having surfaces defined by cutting using a dicer.

Figs. 98A-D of Yasunaga et al. correspond to the disclosure of Japanese Patent Laid-Open No. 4-207046. In JP '046, the seal resin is formed by coating a semiconductor wafer using a spinner. As such, no compression molding is performed.

The physical properties of a compression-molded resin layer and a dispensing method, such as that disclosed by JP '046 as illustrated in Figs. 98A-D of Yasunaga et al., have already been set forth in the paper submitted with the response filed January 18, 2002 (***Kawahara, T., IEEE Trans. Advanced Packaging, vol. 23, no. 2, May 2000, pp. 215-219***). The data contained in that paper is included in the attached declaration of Toshimi Kawahara, one of the co-inventors of the present application and the author of the IEEE paper.

Claims 109-112, 131, 134 and 135 were rejected under 35 USC §103(a) as being unpatentable over Yasunaga et al. further in combination with Kitaura et al. This rejection is respectfully traversed.

The Examiner's statement at lines 3-5 on page 5 of the Office Action supports applicants' argument that Yasunaga et al. fails to anticipate a compression-molded resin layer. Kitaura et al. is applied by the Examiner for its disclosure of a transfer/injection molded resin layer and a compression molded resin layer.

Kitaura et al. merely sets forth that a resin encapsulation is preformed using a thermosetting resin moldable material such as an epoxy resin composition, etc., by casting, compression molding,

injection molding, transfer molding, etc., in particular, by transfer molding which is excellent in mass producibility and workability. It is respectfully submitted, however, that this disclosure does not state that the physical or structural properties are equivalents. Accordingly, Kitaura et al. fails to provide the teachings which Yasunaga et al. lacks, as discussed in detailed above.

Claims 115, 116, 119 and 120 were again rejected under 35 USC §103(a) as being unpatentable over the combination of Karnezos and Yasunaga et al. This rejection is respectfully traversed.

The Examiner incorrectly characterizes Karnezos as providing a resin layer 42c formed on a semiconductor element so as to seal protruding electrodes except end portions thereof. Karnezos does not provide any teaching of such a structure. The protruding electrodes 16c (as characterized by the Examiner) are not at all sealed by the resin 42c. Karnezos clearly states that a "via 44c is formed in second insulating layer 42c to the conductive layer 40c, and a conductive trace 46c is deposited over the surface of the insulating layer 42c within via 44c" (column 5, lines 45-48). Since the conductive trace 46c is deposited within via 44c, it would not be possible for the insulating layer 42c to seal the protruding electrodes except end portions thereof. Karnezos further clearly states what constitutes the button 16c (protruding electrode) at column 5, lines 49-52 as follows: "The button 16c includes a polyimide core 18c and a metallic coating 20c." Thus, for at least these reasons, the rejection should be withdrawn since the combination of references fails to teach all the features of the claimed invention.

Furthermore, claim 115 requires "a part of said protruding electrode sealed by said resin layer and said end portions are covered commonly with said electrically conductive film." The protruding electrodes of the claimed invention are defined as having a core portion and an electrically conductive film formed on a surface of the core portion. As stated by Karnezos, the protruding electrode (button

16c) does not include the trace 46c. Thus, the combination of references also fails to teach these features of the claimed invention.

Independent claim 119 distinguishes over the combination of Karnezos and Yasunaga et al. for at least the same reasons discussed above. Favorable reconsideration and withdrawal of the rejection are earnestly solicited.

Claims 123, 127, 129 and 130 were rejected under 35 USC §102(b) as being anticipated by Brooks et al. This rejection is respectfully traversed.

Independent claim 127 includes features of a compression-molded resin layer formed on a semiconductor element so as to seal the protruding electrodes except end portions thereof, wherein the compression-molded resin layer and the semiconductor element have surfaces defined by cutting using a dicer.

Brooks et al. does not teach or suggest a compression-molded resin layer. Brooks et al. merely teaches encapsulation which may comprise known materials such as siloxane polyimide and epoxy novolac based materials. Accordingly, reconsideration and withdrawal of the rejection are earnestly solicited.

Claims 132 and 133 were rejected under 35 USC §103(a) as being unpatentable over Brooks et al. This rejection is respectfully traversed.

Claim 132 requires that the first and second resin layers be formed of a compression-molded resin layer. There is no suggestion provided by Brooks et al. of a compression-molded resin layer. Furthermore, as noted above, a compression-molded resin layer has different physical and structural properties as compared with a resin layer such as an encapsulation disclosed by Brooks et al.

Claims 123, 127, 129, 130, 132 and 133 were rejected under 35 USC §103(a) as being unpatentable over Brooks et al. further in combination with Kitaura et al. This rejection is respectfully traversed.

The Examiner acknowledges that Brooks et al. discloses a casting molded "gravity leveling" resin layer. Kitaura et al. is applied by the Examiner for allegedly rendering such a layer equivalent with a compression-molded resin layer. However, Kitaura et al. does not disclose that such resin encapsulation provides the same properties, but merely states different methods of resin encapsulation. As evident from the paper from IEEE Transactions on Advanced Packaging, the physical properties are distinct.

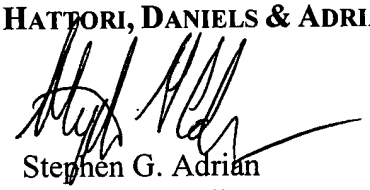
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



Stephen G. Adrian
Attorney for Applicants
Registration No. 32,878

Attachments: Petition for Extension of Time
Declaration under 37 CFR §1.132
Notice of Appeal

SGA/arf
1250 Connecticut Avenue, NW
Suite 700
Washington, D.C. 20036
(202) 822-1100